

09/27/1991

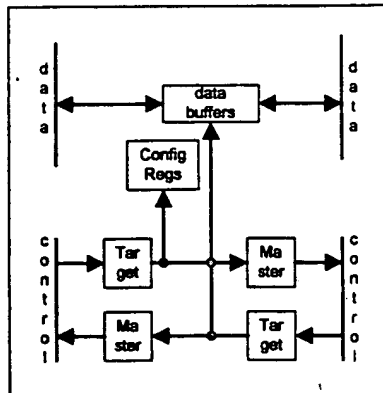


Fig. 1 PCI-PCI Bridge Block Diagram

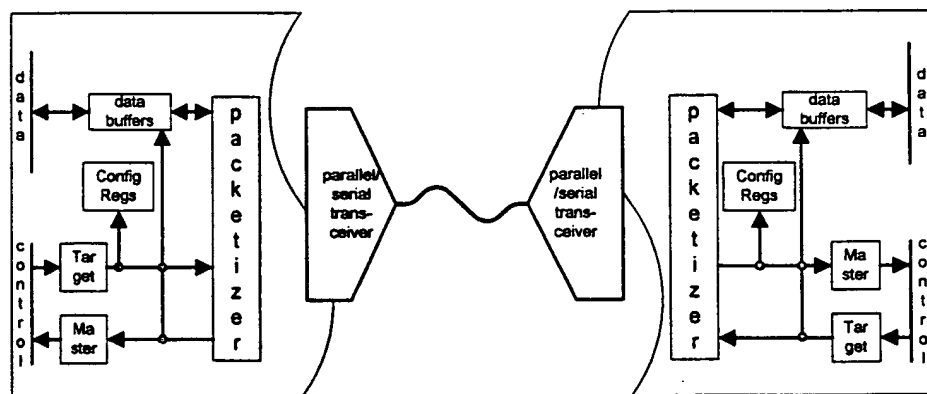


Fig 1A Block System Diagram

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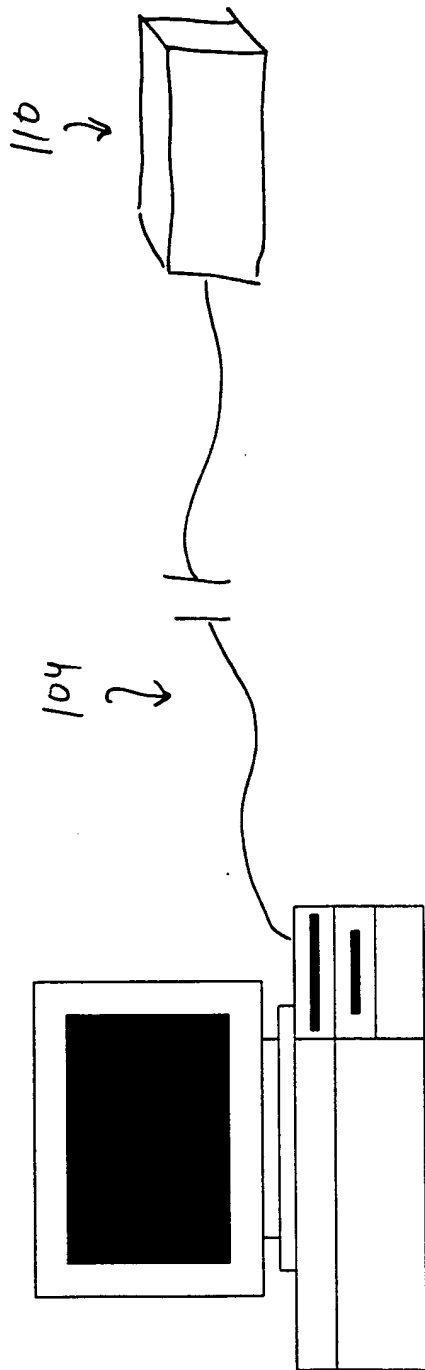


Figure 2

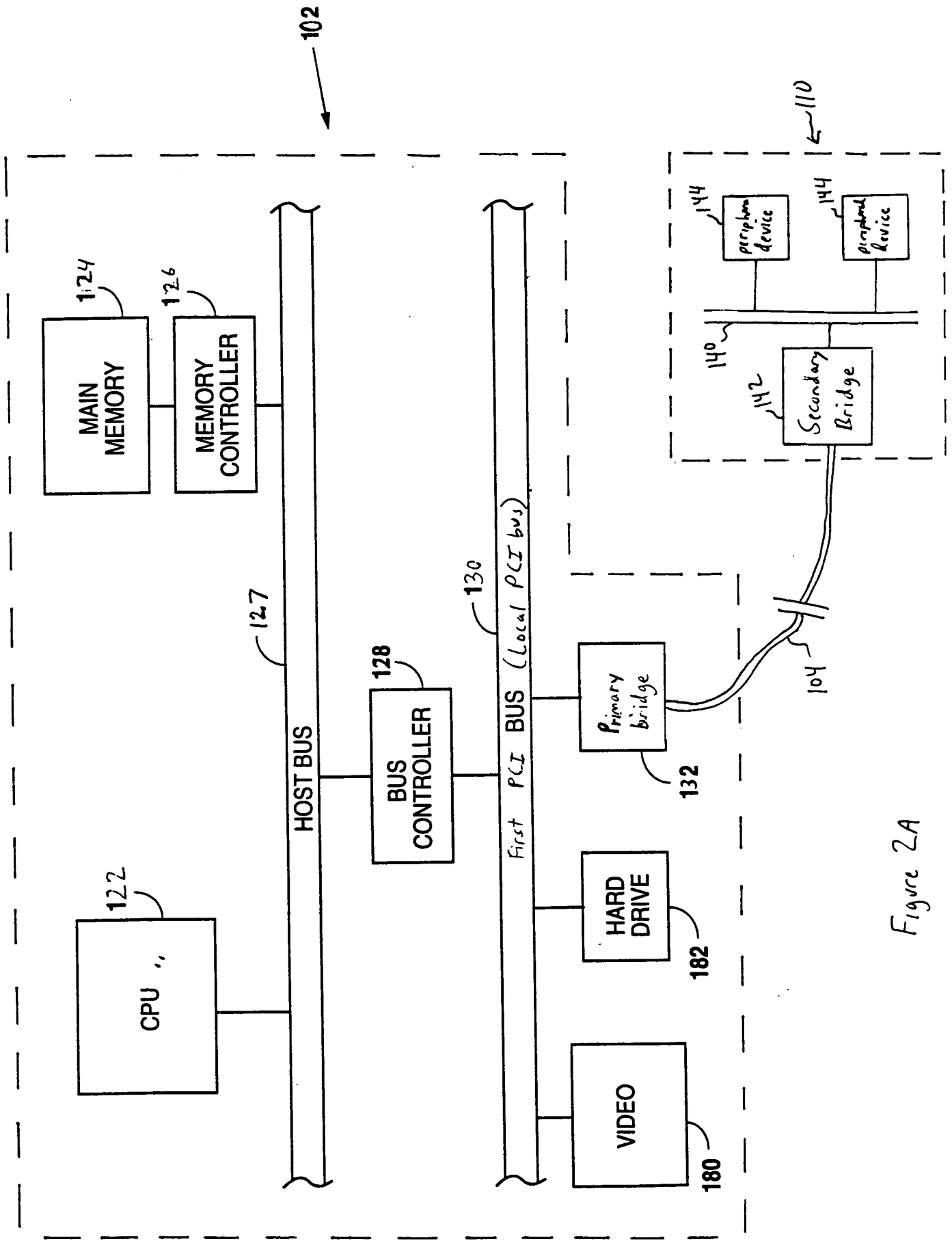


Figure 2A

092460-1697260

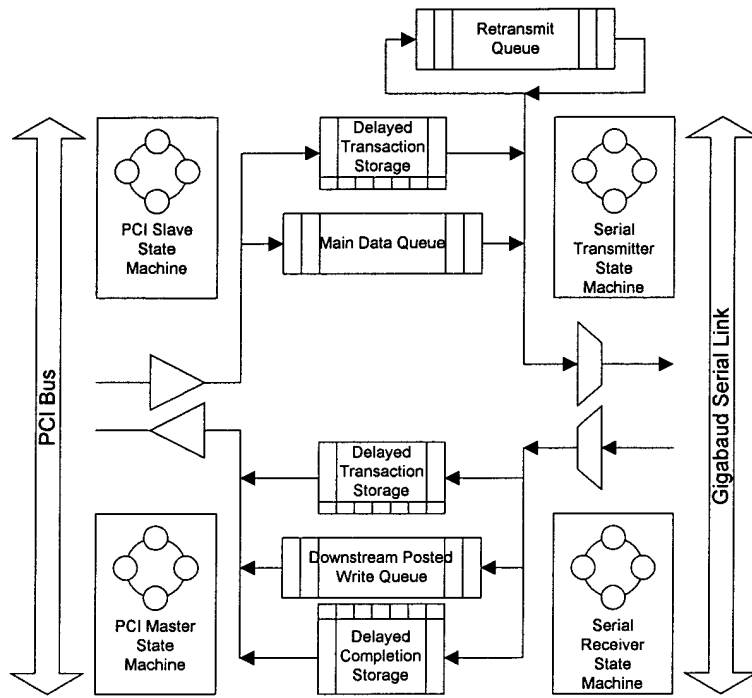


Fig. 3 WASP Block Diagram

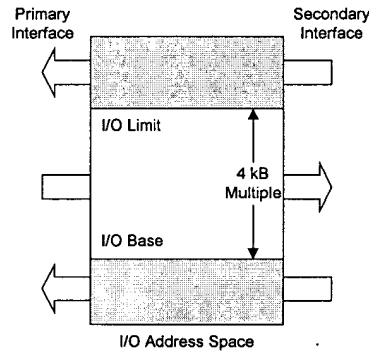


Fig. 4 I/O Transaction Forwarding Map

03274691-03499

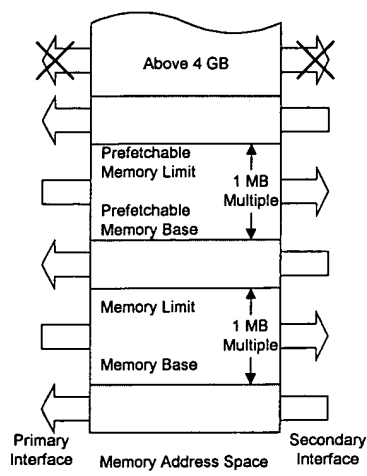


Fig. 5 Memory Transaction Forwarding Map

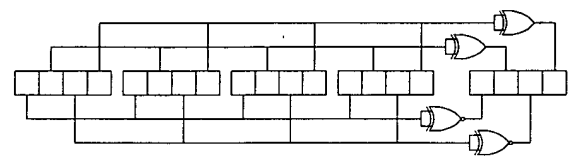


Fig. 6 WASP Frame Format and Parity Generation

Description		17	16	15 12	11 8	7 4	3 0
Posted Write	PW	U	ParErr	1000	PCI Cmd	PCI BE	Par
PCI Configuration	PCR	U	ParErr	1001	PCI Cmd	PCI BE	Par
Delayed Request 0	DR0	U	ParErr	1100	PCI Cmd	PCI BE	Par
Delayed Request 1	DR1	U	ParErr	1101	PCI Cmd	PCI BE	Par
Delayed Request 2	DR2	U	ParErr	1110	PCI Cmd	PCI BE	Par
Delayed Completion	DC	U	ParErr	1111	PCI Cmd	PCI BE	Par
Success Ack	SA	U	U	0001	U	U	Par
Failure Ack	FA	U	U	0010	U	U	Par
Sanity Check	SC	U	U	0011	U	U	Par
Reset	RST	U	U	0100	U	U	Par
Power On	POP	U	U	0101	U	U	Par

Fig. 7 Command Packets

Error Condition	Response
Bad PAR on title frame of command packet	ignore transfer
Bad PAR on packet count frame of command packet	submit Failure ACK if received packet is not a Failure ACK or a Sanity Check
Bad PAR on data packet	submit Failure ACK
Receipt of data packet after fill frame (i.e. command packet did not start transfer)	ignore rest of transfer
Received packet count does not match packet counter	submit Failure ACK

Fig. 8 Error Condition Responses

00	Command Frame
01	PCI Address Frame or Regular Data Frame
10	PCI Data Frame
11	Reserved

Fig. 9 RTQ Packet Encoding

09271691.034899

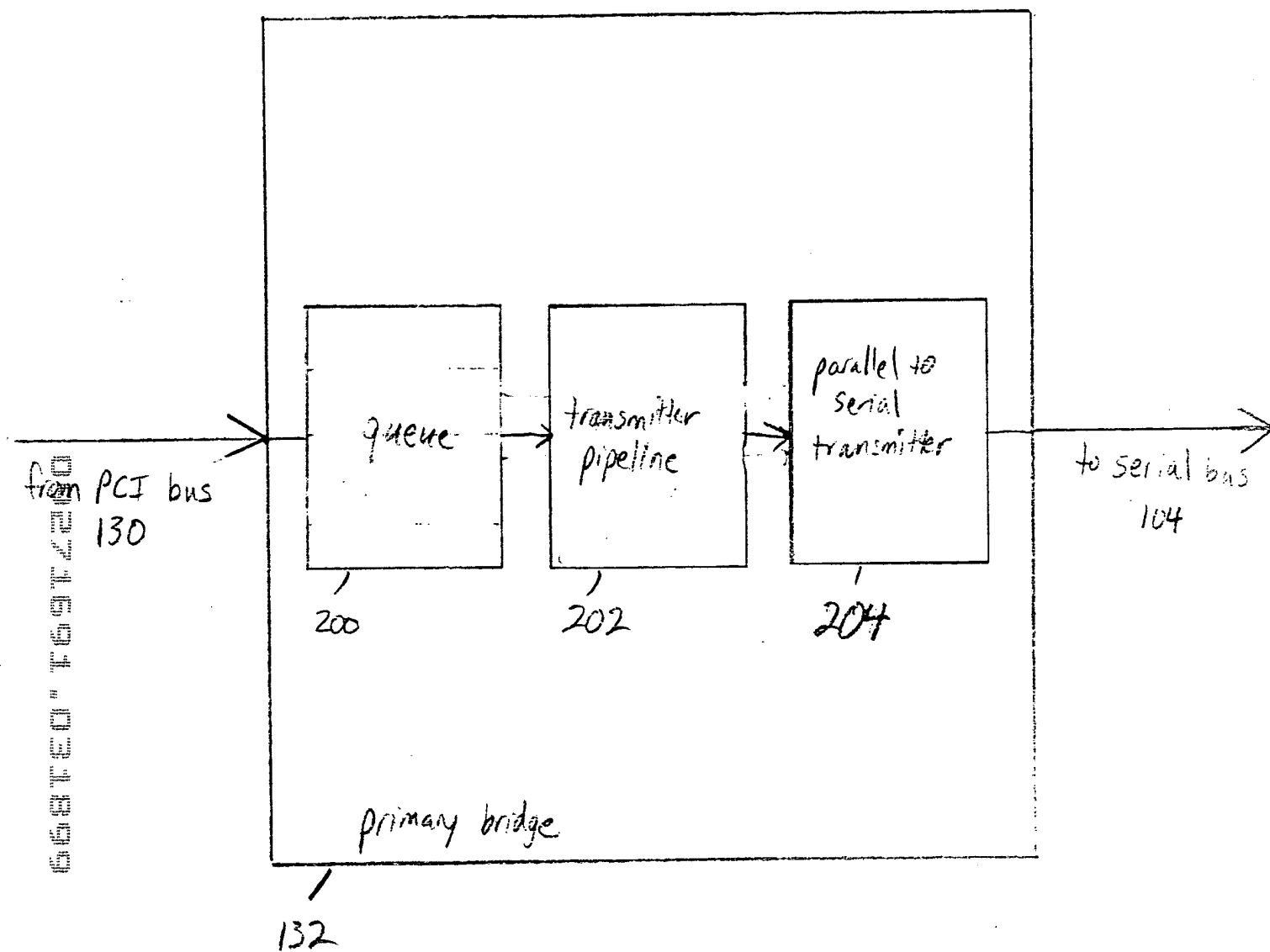


Fig. 10

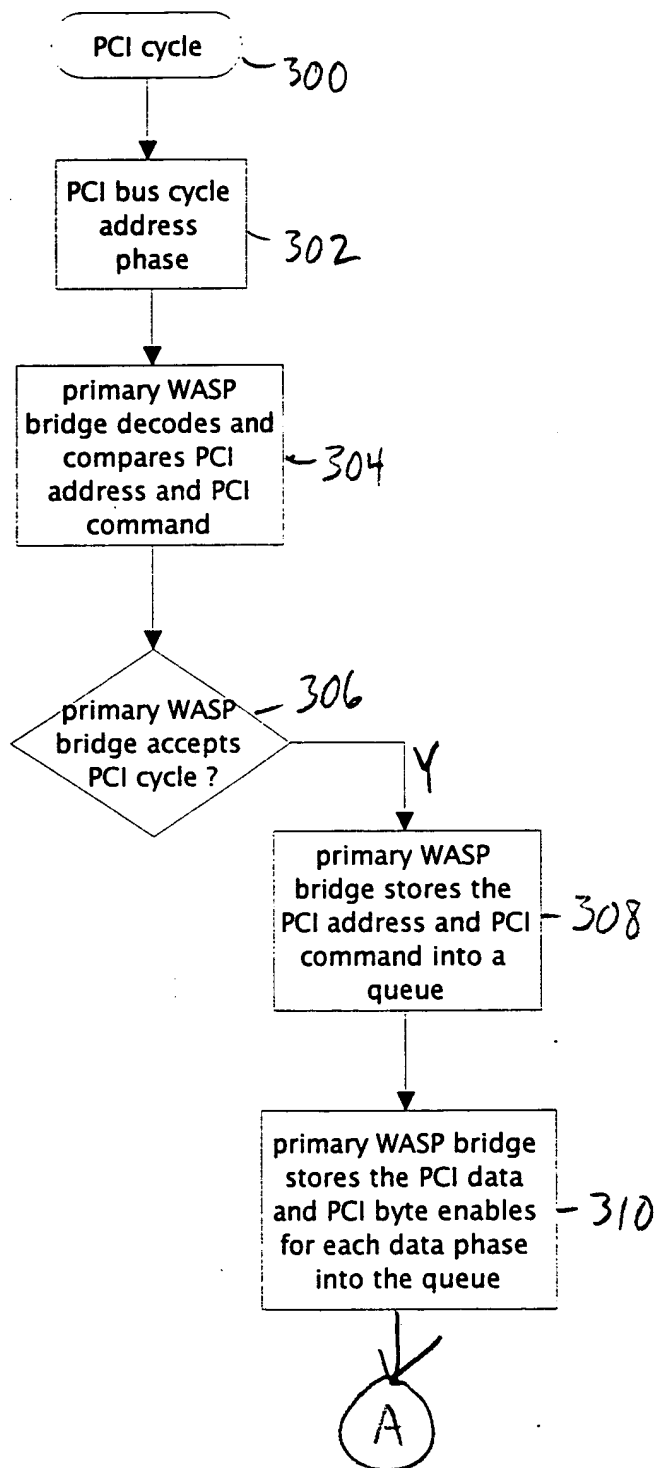


Fig. 11a

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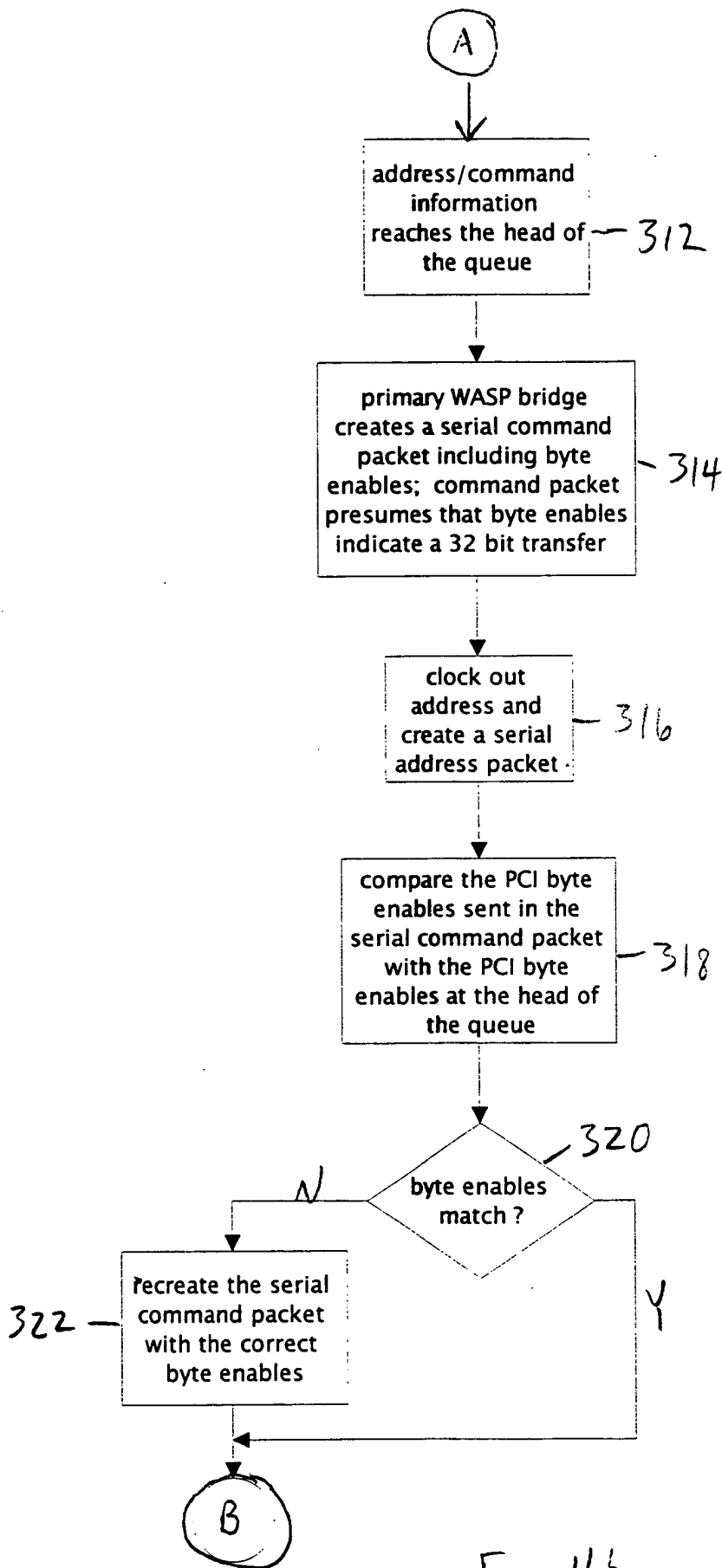


Fig. 11b

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068TE0 T69T260

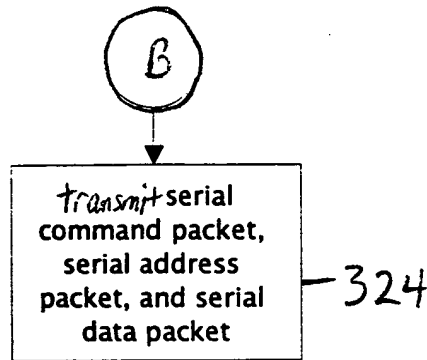


Fig. 11c